Section II (Remarks)

Claims 1-34 are pending in the application.

In the March 23, 2007 final Office Action, the rejection of claims 14-34 was maintained. Claims 1-12 remain withdrawn from consideration. Rejoinder of claims 1-13 upon allowance of claims 14-34 is requested.

Rejection of Claims 14-34 Under 35 USC §103

In the March 23, 2007 Office Action, claims 14-34 were rejected under 35 USC §103(a) as being unpatentable over Reid (U.S. Patent No. 6,458,262) in view of Etherington (U.S. Patent No. 6,231,743).

The examiner in his statement of rejection has contended that:

- the further recital of the computational module introduced to claim 14 in applicants' December 15, 2006 Response is taught in Reid in view of Etherington
- Etherington (at col. 2, lines 30-34 and col. 4, lines 6-6) discloses a control array and a sensing array that are coupled with a computational module that "meets the claimed limitation;" and
- Etherington discloses plating current as an electrode parameter of the wafer-based independent variable (col. 2, lines 25-34) and an electrochemical deposition system arranged with the wafer being plated constituting a cathode element of the electrochemical cell (col. 1, lines 21-21, Fig. 1, and col. 4, lines 49-65).

The examiner additionally has characterized applicants' prior arguments as unpersuasive, on the following grounds:

- as to applicants' argument that Etherington teaches away, the examiner contended that Etherington teaches that the cathode and wafer are coupled by at least a seed layer (col. 4, lines 49-65);
- as to applicants' arguments that Etherington teaches a sensing unit as part of the plating system's diffuser plate, the examiner contended that the sensing unit is still related to a

computation module that controls/monitors and electrode parameter (plating current) as a wafer-based independent variable; and

- as to applicants' arguments that Reid does not specifically disclose a computational module capable of controlling an electroplating process via a wafer-based independent variable, the applicants' arguments are an attempt to differentiate by attacking the references individually whereas the rejections are based on the combinations of the references.

Applicants vigorously traverse the examiner's rejection. Applicants are not seeking to attack the references individually, but are showing that the individual aspects selected by the examiner for combination do not in fact provide a derivative basis for applicants' claimed invention.

In considering a reference for its effect on patentability, the reference is required to be considered in its entirety, including portions that teach away from the invention under consideration. Simply stated, the prior art must be considered as a whole. **W.L. Gore & Associates, Inc. v Garlock, Inc.**, 721 F.2d 1540, 1550 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984). "It is impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art." **Application of Wesslau**, 353 F.2d 238, 241 (C.C.P.A. 1965); **Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve**, 796 F.2d 443, 448 (Fed. Cir. 1986), cert. denied, 484 U.S. 823 (1987).

If a proposed modification of the prior art would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no logical basis for the proposed modification (see **MPEP 2143.01(V)**). As discussed below, no basis for *prima facie* obviousness of the applicants' claimed invention has been established.

Reid is directed to an apparatus and method for the on-line monitoring and control of the electroplating chemistry of an electrochemical deposition system wherein plating bath solution is sampled and evaluated to assess the relative concentrations of the various plating bath components. The system in Reid requires on-line extraction of the plating bath solution, directly

or indirectly, from the plating bath during operation and its subsequent analysis in a coupled chemical analysis system.

The Reid process system includes, by necessity, the removal of the organic components from the other components of the plating solution before its analysis. The computer (computational module) in such system is in electrical communication with the on-line chemical analysis system. The computational module, in response to the analytical data relating to the chemistry of the plating bath solution, then communicates with and regulates the feed valves for the components to the plating bath and the communication bus, which controls the system hardware, for controlling the whole of the electroplating system and its operation.

The Reid system embodies an apparatus and process of the type that applicants are specifically endeavoring to replace due to its many shortcomings, namely, an apparatus and process that rely upon the isolated testing and evaluation of the plating bath solution in a coupled but independent analytical apparatus removed from and outside of the electroplating cell itself.

As noted by applicants in their specification, the evaluation of electroplating fluid away from the electroplating cell does not present a real-time status of the system or solution at the wafer – the location at which the plating is taking place. See paragraph [0005] of the present specification:

> [0005] Current methods of analysis of components of the ECD plating bath include high pressure liquid chromatography (HPLC), cyclic voltametric stripping (CVS) and pulsed cyclic galvanostatic analysis (PCGA). Each of these monitoring techniques requires expensive hardware that uses valuable cleanroom space, and is susceptible to downtime resulting from monitoring system malfunction or failure, or from periodic maintenance requirements. In addition to such cost and reliability issues, none of these conventional techniques provides a true and accurate indication of the deposition process on the substrate that is being metallized.
>
> (Emphasis added)

The applicants have overcome such deficiency of the prior art by providing an on-wafer metrology apparatus and process. Such on-wafer apparatus and operation are nowhere disclosed in or derivable from the combination of Reid and Etherington.

The computational module of Reid is constructed and configured for receiving and analyzing data from the chemical analysis system, conducting computations relative to such data, and subsequently issuing instructions to other components of the electroplating system for ensuring/achieving the desired plating.

Reid does not involve a wafer-based variable or an apparatus wherein the wafer itself is both the cathode of the plating operation as well as the sensor for monitoring of the plating operation.

Etherington in combination with Reid does not overcome such deficiency of the Reid reference.

Etherington discloses a method of forming a semiconductor device wherein the electroplating operation is monitored and controlled by sensing arrays and control arrays that are incorporated in the plating chamber, intermediate the substrate to be plated and the anode. The sensing arrays of Etherington are electrical sensors whose function is limited to measuring current flowing through the electroplating solution from the anode to the cathode.

Specifically, the sensors are designed to sense and detect changes in current flow across a cross-sectional plane in the electroplating fluid bath. This plane is perpendicular to the flow of the plating solution within the plating cell itself, at any given point in time.

In response to any detected current flow variations in the Etherington system, adjustments may be made in the current flow or voltage potential in the affected region to provide the proper and desired rate of plating.

Contrary to the assertion of the examiner, the wafer in the Etherington system is neither employed as nor acts as a sensor. In addition, Etherington does not monitor or employ a wafer-based variable.

Accordingly, Etherington fails to provide any logical basis for a computational module

> "being adapted for coupling in signal processing, monitoring and control relationship with the electrochemical deposition system when said electrochemical deposition system is arranged with the wafer being plated constituting a cathode element of an electrochemical cell including said copper plating anode, and said computational module being arranged to process an electrode parameter of said wafer as said wafer-based independent variable in said regression analysis" (emphasis added),

as required by applicants' claimed invention.

Indeed, despite the examiner's contention that Etherington teaches its sensing array as being coupled to the cathode and the wafer (seemingly inferring that the wafer and the sensor array are, or can be, one and the same), Etherington only allows for physical coupling so as to have one in close proximity to the other.

Etherington very clearly and specifically discloses that the sensing array and the cathode are not electrically connected (see col. 4, lines 6-9). See also Etherington's claims, reiterating the requirement that the monitoring of the current is at a place "**apart from** the cathode and anode and the substrate within the plating bath" (claim 1) or at a place "**apart from and between** a cathode and an anode associated with the plating bath (claim 11).

Despite the examiner's assertion that the Etherington computational module could be employed in substitution for the Reid computational module (paragraph 8, September 15, 2006 Office Action), there is no disclosure in either reference supporting such substitution, and no logical basis on which one skilled in the art could infer such an arrangement from Reid in view of Etherington.

The examiner's "could be employed" basis for obviousness of combining Etherington with Reid is legally improper and has been expressly discredited in numerous controlling decisions. See **In re Rouffet**, 149 F.3d 1350, 1357 (Fed. Cir. 1998); **In re Mills**, 916 F.2d 680, 682 (Fed. Cir.

1990) ("The fact that references **can be** modified or combined is **insufficient to meet this criterion [of obviousness]**" (emphasis added)).

Nothing in Etherington describes or evidences the existence of a computational module. The text in Etherington cited by the examiner, at column 2, lines 16-34, speaks of monitoring the current and, in response thereto, adjusting the bath flow rate and bias potential. Nothing more is disclosed.

The Etherington description is consistent with monitoring and operation by a human technician, involving manual operation, or use of mechanical, pneumatic, electrical, electropneumatic, or other process components.

The examiner therefore is attributing to Etherington disclosure and significance that simply is absent from such reference.

Even if Etherington were somehow construed to disclose the presence of a computational module, although no basis exists for such construction, the substitution of such a hypothetical computational module for that of Reid would not be feasible and the attempted synthesis would render Reid inoperative for its intended purpose.

As noted above, the computational module of Reid is designed and configured to (i) receive data from an on-line chemical analysis of the electroplating bath solution, (ii) compare that data to certain standards and, subsequently, (iii) make adjustments to the plating bath chemistry and/or current, to provide for an efficacious plating process.

Etherington, on the other hand, employs an array of sensors to measure variance in current flow across a cross-section of the plating bath solution. This is not a measurement of changes in current with time but rather a simultaneous measurement to identify pockets within the fluid of different current flow or strength at a specific point in time.

In Etherington, when sensors detect differences in the current flow, various control means are used to adjust the current in those regions of the bath solution corresponding to the location of

the sensor registering the different current flow, in order to achieve the desired rate of plating at the corresponding location on the wafer or substrate. This sensor arrangement, however, has no value if the plating bath solution is depleted of the proper constituents or if the concentration of such constituents is inconsistent with, or insufficient to achieve, the desired plating operation.

The objectives and character of the systems of each of Reid and Etherington are different and neither is compatible with or complimentary to the other.

Reid involves an electrochemical analysis of its plating bath solution so as to monitor the depletion of its constituents and make adjustments in the same to ensure that the proper levels are present.

Etherington merely monitors current flow across and at distinct points in the plating bath solution flow stream and, consequently, makes adjustments in the current flow and/or voltage potential at those distinct points, or in the overall plating solution flow rate, in order to adjust the rate of plating at the corresponding surface of the wafer or substrate to be plated, to a desirable value.

Etherington is neither concerned with nor has any means to make any adjustments relative to the actual make-up of the plating solution other than to speed up the rate at which the fluid in the bath is replenished with fluid from the reservoir.

Changing the system and mode of operation of Reid to one that is based on current flow would merely frustrate its purpose.

Reid and Etherington both measure variables in the fluid, but they are not the same variables nor are they measured for the same purpose.

Since the two systems are incompatible, and since the proposed combination or substitution would render Reid inoperable and completely frustrate its intended purpose, there is no logical basis for the combination.

Accordingly, no *prima facie* obviousness is present. Reid conducts an actual chemical analysis of the plating solution to measure the concentration of the constituents thereof in order to control the same. Etherington measures the current flow at particular points in the plating bath solution to make adjustments in the current flow at those very points to address anomalies or issues relative to the rate of plating at specific locations on the surface of the wafer or substrate.

In applicants' claimed invention, the wafer itself serves as the sensor feeding various wafer-based parameter values to the computational module. The applicants' computational module is constructed and configured to accept data from the wafer, process the same and then make adjustments in the overall process and process parameters to ensure effective plating – as recited in applicants' independent claim 14, from which all remaining claims 15-34 under consideration are directly or indirectly dependent, the applicants' claimed apparatus requires a "...computational module being arranged to process **an electrode parameter of said wafer** as said wafer-based independent variable..." (emphasis added). This feature is absent from and cannot be derived from the combination of Reid and Etherington.

Contrary to the examiner's assertion, neither reference contemplates or even allows for an electrode or the wafer serving as the sensor, and neither reference discloses or contains any derivative basis for an electrode based parameter, let alone a wafer-based parameter, as the input to the computational module.

The applicants' claims 14-34, requiring, *inter alia*, a

> "computational module being adapted for coupling in signal processing, monitoring and control relationship with the electrochemical deposition system when said electrochemical deposition system is arranged with **the wafer being plated constituting a cathode element of an electrochemical cell including said copper plating anode**, and said **computational module being arranged to process an electrode parameter of said wafer as said wafer-based independent variable in said regression analysis,**"

are therefore patentable over the art.

The recent U.S. Supreme Court decision in KSR International Co. v. Teleflex Inc., 550 U.S. ___ (2007) does not change this result. Although that case held that the teaching, motivation or suggestion test should not be strictly applied in determining obviousness, it remains true that there must be a reason in logic and fact for combining references, and that references that teach away from the invention are evidence of the non-obviousness of a claimed invention. Under pre-KSR or post-KSR standards - the combination of Reid and Etherington fails to render the applicants' claims obvious. The Supreme Court in KSR reaffirmed the Graham factors, and Graham analysis compels the conclusion that the applicants' claims are not obvious and merit allowance.

It is fundamental to a proper 103 rejection of claims that an examiner must present a convincing line of reasoning supporting the rejection. MPEP 2144 ("Sources of Rationale Supporting a Rejection Under 35 U.S.C. 103"), citing *Ex parte Clapp*, 227 USPQ 972 (Bd. Pat. App. & Inter. 1985). The Supreme Court in KSR affirmed the validity of such approach, stating that "there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." The Court also reaffirmed the principle that a factfinder judging patentability "should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon ex post reasoning."

Here, there is nothing in the combination of cited references that additively, permutatively or extrapolatively yields the applicants' claimed invention, comprising a

> "computational module being adapted for coupling in signal processing, monitoring and control relationship with the electrochemical deposition system when said electrochemical deposition system is arranged with **the wafer being plated constituting a cathode element of an electrochemical cell including said copper plating anode**, and said **computational module being arranged to process an electrode parameter of said wafer as said wafer-based independent variable in said regression analysis,"**

as required by applicants' claimed invention.

Claims 14-34 are patentable, and merit allowance.

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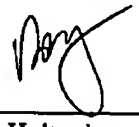
CONCLUSION

Based on the foregoing, applicants' pending claims are patentably distinguished over the art, and in form and condition for allowance. The examiner is requested to issue a Notice of Allowance. If any matters require further resolution, the examiner is requested to contact the undersigned attorney at (919) 419-9350 to discuss same.

Respectfully submitted,



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